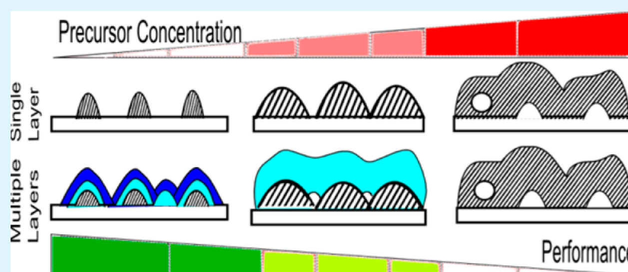
High Mobility Indium Zinc Oxide Thin Film Field-Effect Transistors by Semiconductor Layer Engineering

Daniel E. Walker,*[†] Marton Major,[‡] Mehrdad Baghaie Yazdi,[†] Andreas Klyszcz,[§] Marc Haeming,[§] Klaus Bonrad,[§] Christian Melzer,[†] Wolfgang Donner,[†] and Heinz von Seggern[†]

[†]Technical University of Darmstadt, Department of Materials Science, 64287 Darmstadt, Germany
[‡]WIGNER RCP, RMKI, H-1525 Budapest, P.O.B. 49, Hungary
[§]Merck TU-Darmstadt Laboratories, 64287 Darmstadt, Germany

Supporting Information

ABSTRACT: Indium zinc oxide thin-film transistors are fabricated via a precursor in solution route on silicon substrates with silicon dioxide gate dielectric. It is found that the extracted mobility rises, peaks, and then decreases with increasing precursor concentration instead of rising and saturating. Investigation with scanning probe techniques reveals full thickness variations within the film which are assumed to adversely affect charge transport. Additional layers are coated, and the extracted mobility is observed to increase up to 19.7 $cm^2\ V^{-1}\ s^{-1}$. The reasons for this are examined in detail by direct imaging with scanning tunneling microscopy and extracting electron density profiles from X-ray reflection measurements. It is found that the optimal concentration for single layer films is suboptimal when coating multiple layers and in fact using many layers of very low concentrations of precursor in the solution, leading to a dense, defect and void free film, affording the highest mobilities. A consistent qualitative model of layer formation is developed explaining how the morphology of the film develops as the concentration of precursor in the initial solution is varied.



KEYWORDS: *thin-film transistor, solution process, multilayer, morphology, density, porosity*

1. INTRODUCTION

Indium zinc oxide (IZO) thin-film transistors offer a wide variety of potential advantages compared to amorphous silicon and organic devices, including high mobilities, solution processability, environmental friendliness, and relatively low temperature processing.[1] The display industry, which has traditionally used amorphous-Si as the material of choice to fabricate backplane electronics, requires materials with considerably higher charge carrier mobilities such as poly-crystalline silicon for use in next generation fast refresh rate, high-resolution liquid crystal (LC), and organic light-emitting diode (OLED) displays.[2] However, poly crystalline silicon requires many processing steps and as such is considerably more expensive and also inherently unstable due to its inhomogeneous grain structure. Nomura et al. highlighted the potential of indium gallium zinc oxide (IGZO) in 2004, and since then, doped indium oxides have become materials of considerable interest and have started to be used in commercial display products, albeit deposited by expensive processes like chemical vapor deposition or sputtering.[3] Recently, solution processable metal oxide formulations have been shown exhibiting the potential to reach the required high mobilities and stability to be a candidate for poly crystalline silicon replacement.[1] Using multiple layers to improve device performance has so far only been touched upon in literature, where Wang et al. have previously investigated coating solutions of different concentrations of zinc oxide (ZnO) to create multilayer films and noticed a modest improvement depending on the order the layers are coated.[4] They also reported that the surface roughness plays a critical role in the ultimate performance but offered no sufficient explanations for these observations. Similarly, Theissmann et al. noticed a doubling in device performance when coating a second layer of ZnO from solution, and Tellier et al. showed that the conductivity of multiple layer ZnO films improves, while the surface roughness decreases.[5,6] Further studies have focused on transparent conducting oxides and on approaches to improve the conductivity by coating layers of different materials or doping levels; however, explanations describing what is happening on a morphological level and why the additional layers improve the films over coating single, thick layers, are absent.[7−9] Furthermore, it has been reported in the literature that sol−gel deposited IZO films are amorphous and do not suffer from grain boundaries that are thought to cause inhibited performance in zinc oxide.[1,10] Only very recently, a first report has been published implying that the morphology of a

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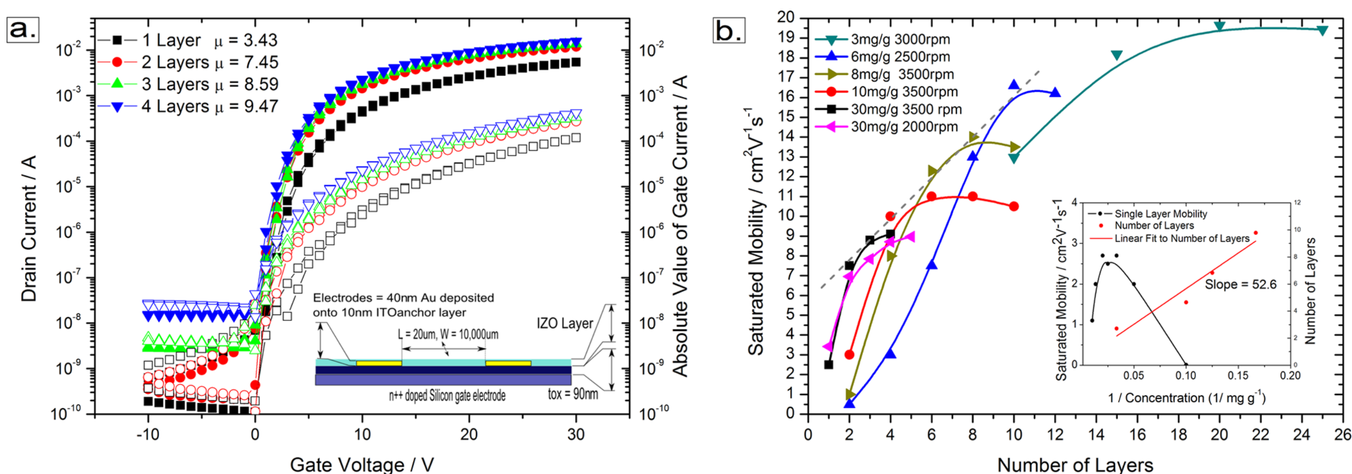

Figure 1. (a) Transfer characteristics of devices in the linear regime for different numbers of layers. The drain current (filled symbols) for both forward and reverse sweeps are shown as is the gate current (open symbols). Inset: Details the device geometry (b). The saturated mobility plotted against the number of layers for various spin coated devices. Inset: 1/concentration vs saturated mobility of precursor in solution for single layer devices and 1/concentration vs number of layers from the osculation point of the trend line shown in the main figure (dashed line).

semiconducting oxide layer is critical to device performance and that this performance can be moderately improved by coating multiple layers where a mobility increase from 1.2 $cm^2V^{-1}s^{-1}$ for a single layer to 2.8 $cm^2V^{-1}s^{-1}$ for two layers is reported.[11] The authors also report a linear thickness increase with the number of layers deposited and postulate that the lower layer has voids filled in by the upper layers.

In the present paper, it is shown that, while this picture may be close to correct for thicker layers, it is incomplete, and far greater gain can be made by understanding how the layer initially forms by utilizing very low concentration solutions of precursors, resulting in devices with an order of magnitude increase in performance, over those shown by Kim et al.[11] with values up to around 20 $cm^2V^{-1}s^{-1}$. X-ray reflectivity measurements are used to quantitatively extract the density as a function of film thickness and STM employed to produce high resolution images of the surface, affording a full understanding of the films growth mechanisms and the development of the films morphology as multiple layers are added. Further improvement will be gained by tuning the concentration of precursor to result in a thin but void free film giving the best performance. This approach is taken to its logical conclusion of attempting ever thinner layers presenting a full study on the effect of precursor concentration when coating multiple layers.

2. EXPERIMENTAL SECTION

In all experiments described, a highly doped (n++, $n \sim 3 \times 10^{17}$ cm^{-3}) silicon substrate with a 90 nm surface oxide layer and optional 30 nm Au source and drain electrodes deposited on top of a 10 nm ITO anchor layer, patterned via a lift off technique, have been used. The substrates were purchased from Fraunhofer Institut Photonische Mikrosysteme, Dresden, and the schematic structure is shown in the inset of Figure 1a. The substrate was cleaned by ultrasonication in acetone to remove a polymer protection layer and, subsequently, in water, acetone, and propane-diol for 10 min each to obtain a clean and residue free surface. The substrates were dried in a flow box for at least 1 h before being plasma treated for 1 min in an air plasma induced by a PFG300RF generator at 70W which significantly improves the wetting of the precursor formulation to the substrate.

Indium zinc oxide (IZO) precursor formulations were prepared from solutions of organo-metallic zinc oximate precursor or indium oximate precursor complex detailed in refs 12 and 13, respectively, dissolved in 2-methoxyenthanol (Aldrich anhydrous 99.8%) and mixed in a 1.66:1 molar ratio of indium to zinc at an optimum single layer concentration of 30 mg of precursor in a total of 1.0 g of solvent and precursor mixture (30 mg g^{-1}). This formulation was spin coated onto the substrate at 2000 rpm for 30 s which was subsequently placed onto a hot plate in air at 450 °C for 10 min in order to decompose the precursor and form the metal-oxide layer. It was then quench cooled to room temperature on a metal block for 30 s. Subsequent layers can then be coated by the same method.

For electrical measurements, transistor characteristics were measured using an Agilent 4155B or Agilent B1500 semiconductor parameter analyzer. Field-effect mobilities have been extracted in the linear regime (μ_L) as a function of gate voltage (V_g) extracted from transfer characteristics using the transconductance method. Mobility in the saturation regime (μ_S) has been extracted by a linear fit to the $I_d^{1/2}$ data from the transfer characteristic. See Supporting Information and Figure S1 for further details. V_g is varied from −20 to +30 V, and the source-drain voltage (V_{sd}) is held constant at 5 V (linear regime) or 30 V (saturation regime); mobilities are extracted using eqs 1 and 2, respectively:

$$\mu_L \approx \frac{\partial I_d}{\partial V_g} \frac{L}{WCV_d} \tag{1}$$

and

$$\mu_S = \frac{2L}{WC}\left[\frac{\Delta I_d^{1/2}}{\Delta V_g}\right]^2 \tag{2}$$

The transistors have a width to length ratio of 500, and the device capacitance per unit area is calculated from $C = \varepsilon\varepsilon_0$ d^{-1}, where ε_{SiO2} was taken as 3.9 and the thickness of the dielectric was d = 90 × 10^{-9}m.

The different layers have been characterized by scanning tunneling microscopy (STM) and atomic force microscopy (AFM) in non-contact mode with DP15/HiRES-C/AIBS tips, purchased from Micromasch, using an Omicron VT AFM ultrahigh vacuum system (pressure <2 × 10^{-10}mbar). Line profiles and statistics were extracted using Gwyddion software and done so before image enhancing techniques used to create clear visual images could potentially alter the data.

Specular X-ray reflectivity (XRR)[14] measurements were carried out on a Rigaku SmartLab diffractometer using Cu Kα radiation to determine the depth dependent average electron density (ED) of the thin films. XRR is a powerful tool to independently determine the thickness and density of a single layer on a substrate. For arbitrary ED profiles, similarly to X-ray diffraction, the phase information is lost, and

therefore, direct inversion of the reflectivity curves is generally not possible.[15] A given reflectivity measurement can, however, be fitted with different ED profiles (see, for example, a recent debate on the interpretation of XRR data).[16−18] For evaluation of the XRR measurements, the GenX software has been used,[19] employing the Parratt recursion algorithm.[14] The instrument dependent parameters were determined from the reflectivity of a bare oxidized Si substrate. The parameter errors are estimated from the 5% increase of the figure of merit (FOM).[20] The ED profiles are interpreted in terms of film thickness, density, and roughness.

3. RESULTS AND DISCUSSION

IZO transistors can be routinely prepared with mobilities of around 3 $cm^2\ V^{-1}\ s^{-1}$ by spin coating a single layer as described in the Experimental Section. A typical transfer characteristic utilizing a precursor concentration of 30 mg g^{-1} in solution is shown in Figure 1a (square data points). The obtained mobilities for single layer devices, for concentrations varied between 5 and 100 mg g^{-1}, keeping the molar ratio (In/Zn) of the precursors constant, are displayed in the inset of Figure 1b (circle data points). It should be noted for clarity that this figure shows the inverse of the concentration, and varying the concentration of precursor in solution translates directly to varying the layer thickness of the deposited layer between 2 and 18 nm. Interestingly, the recorded mobility does not simply increase with concentration or layer thickness but peaks at a concentration of 30 mg g^{-1} which translates to a layer thickness of around 6 nm. Similarly to Kim et al.,[11] the threshold voltage shifts negatively as the concentration is increased from the lowest value until the peak value of 30 mg g^{-1} after which the threshold remains constant at around zero volts. Kim et al. attribute this to a change in charge carrier density, which as calculated is an oversimplification as it does not take into account the changing geometry of the device due to changing the morphology.[11] From the scanning tunneling microscopy (STM) image, shown in Figure 2a, it can be concluded that at the optimum 30 mg g^{-1} concentration the curing of the single layer of the precursor forms a dense worm-like structure of IZO on the silicon dioxide (SiO_2) insulator interrupted by deep trenches or grain boundaries and thickness variations as large as 6.7 nm which is comparable to the total layer thickness as determined by X-ray reflection (XRR) measurements. These deep trenches are also evident in both atomic force microscopy (AFM) and STM surface profiles where the latter are shown in Figure 2d, which show height variations of around 5 nm. Both techniques indicate that areas of IZO free SiO_2 gate insulator surfaces are still present after the first layer deposition. This would lead to significant hindrance of charge flow between source and drain or charge trapping at the defects revealing itself in a more positive threshold voltage, as observed by Kim et al.[11]

At higher concentrations, hence higher layer thicknesses, the measured mobility is reduced as can also be seen from the inset of Figure 1b. This effect can be attributed to a change in morphology.

Since the thickness is increased at higher concentrations, the appearance of voids within the layer becomes more likely. This is presumably due to a faster curing of the surface regions and a resulting intermittent enclosure of solvent and precursor residues in the bulk of the layer. By further curing, the solvent and residues escape from the layer leaving porous voids behind which then form percolated charge transport pathways with weak links between the grains in the transistor channel explaining the observed low mobility values. Note that in a more general view it can be assumed that the reaction kinetics during curing of the film may differ between the surface and the bulk of the film which obviously effects the concentration and diffusion of atoms, clusters, and precursor (fragments). This can be visualized from the scanning electron microscopy images and secondary ion mass spectroscopy data presented in the Supporting Information.

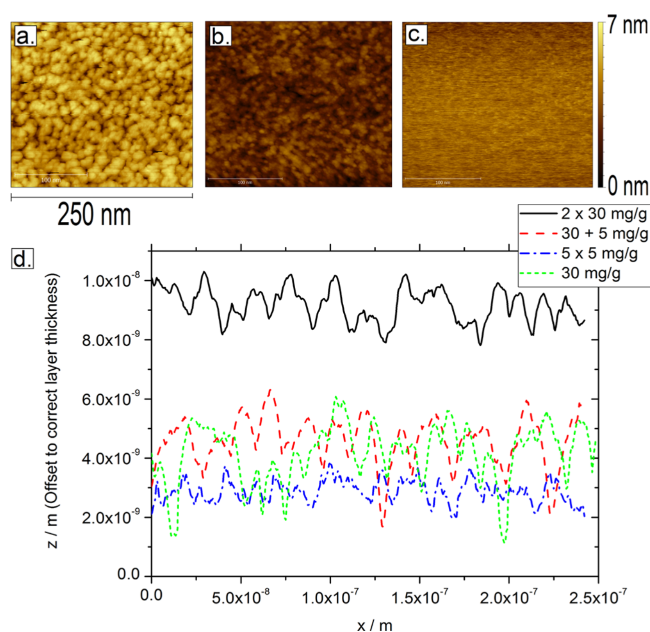

Figure 2. (a) STM image of an IZO single layer made from 30 mg g^{-1} solution. (b) STM image of an IZO two layer sample made from the same solution as (a). (c) STM image of the very smooth 5 × 5 mg g^{-1} layer. (d) Arbitrary line profiles from (a), (b), and (c) showing the multilayer samples are less rough than the single layer. Note: The images (a−c) are all 250 nm wide and have been leveled using Gwyddion software and *z*-scale chosen to be identical with the lowest data point set to 0 nm. The actual data was not altered or scaled in any way.

From the above single layer structures, it was concluded that the surface coverage does not seem to be perfect and that most probably percolation or weak links between grains are limiting the mobility even for the highest mobility values. Therefore, an additional layer with a concentration of 30 mg g^{-1} was deposited on the single layer with the optimal precursor concentration resulting in an approximately 3-fold increase in effective mobility from 2.5 to 7.5 $cm^2\ V^{-1}\ s^{-1}$. The bilayer film has a thickness comparable to a single layer of 60 mg g^{-1}; however, whereas the double-layer device exhibits an increase in mobility, the single layer of 60 mg g^{-1} exhibits a strongly reduced mobility. Coating a third layer results in an additional small increase in effective mobility; however, subsequent layers show no further improvement. The related transfer characteristics are shown in Figure 1a for an increasing number of added layers utilizing the 30 mg g^{-1} precursor solutions. It can be seen that the threshold voltage does not shift significantly with the addition of extra layers but the on-current increases, hinting that the effect is not an increase in free charge carrier density which should produce a threshold shift. It should be noted here that the gate current, hence off current, is shown to increase with the additional layers and to be generally high although below 0.01 of the drain current in the on regime. This is a consequence of the geometry of the device, where the substrate itself forms the gate electrode and spin coated material coats to

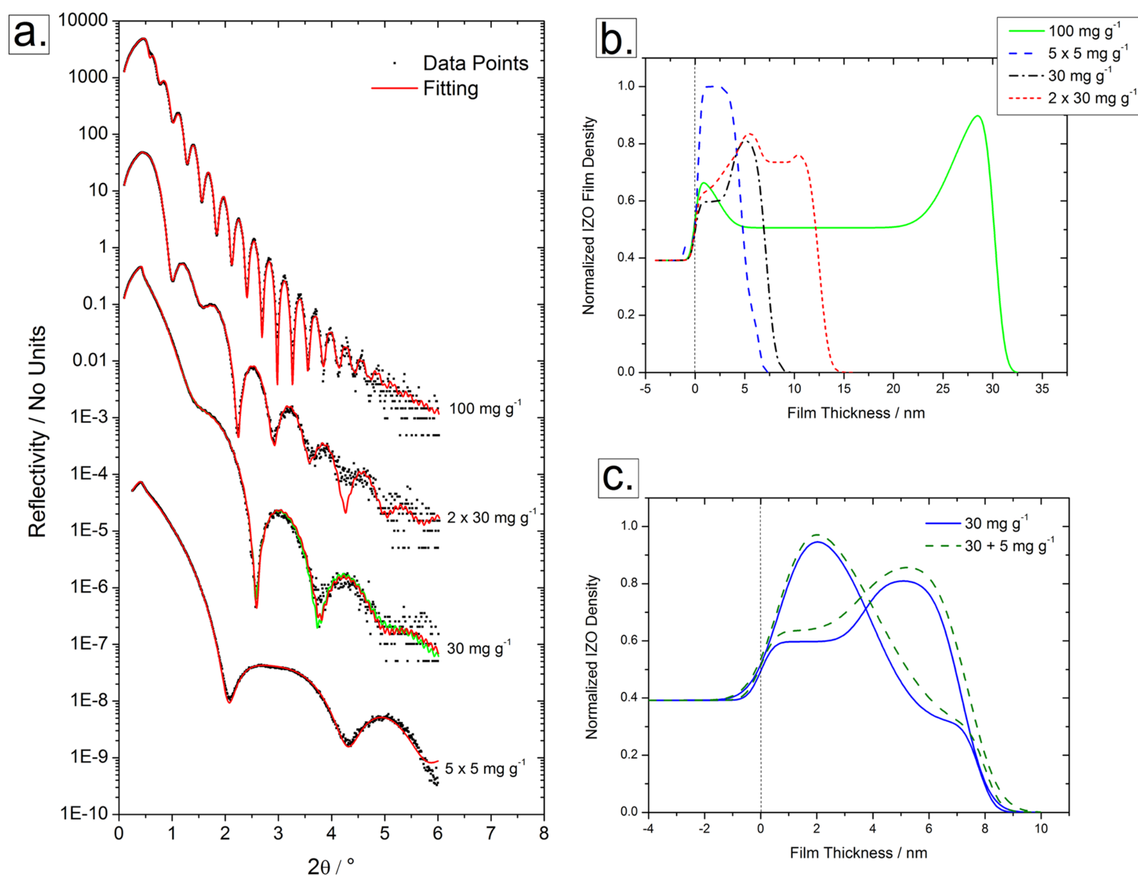

Figure 3. (a). The XRR of the 5 × 5, 30, 2 × 30, and 100 mg g^{-1} samples (from bottom to top). The curves are shifted for clarity. Points show measurement data; lines display the fitting. For the 30 mg g^{-1} single layer sample, two different ED profiles gave almost the same result (bottom of the layer denser: red; top denser: green). (b). ED of the films normalized to the bulk ED (1.7846 el $Å^{-3}$) of IZO with the molar ratio In/Zn = 1.66: 1 of the samples 30, 2 × 30, 100, and 5 × 5 mg g^{-1}. The zero point of the depth scale is at the surface of the oxidized substrate. (c). ED fits of the 30 mg g^{-1} and 30 + 5 mg g^{-1} films with the bottom denser (i) and top denser (ii) models.

the edge of the substrate affording a relatively efficient current path to the gate.

The result for the mobility as a function of the number of layers for different precursor concentrations is displayed in Figure 1b. It is clearly visible that the mobility saturates with a finite number of layers at a value which increases with the inverse of the utilized precursor concentration up to a peak value of 19.65 cm^2 V^{-1} s^{-1} for the 3 mg g^{-1} sample, which is comparable to values obtained by sputtered IZO films.[21] Lowering the concentration further does not result in further gains in performance and requires more layers to reach peak performance as expected if there is no change in film morphology. One can visualize from Figure 2a−c the effect of additional layers on the structure and from Figure 1b the change in performance. Coating a second 30 mg g^{-1} (Figure 2b) layer results in a total layer thickness of about 12 nm which corresponds to approximately double the single layer thickness while the surface roughness is decreased from 0.71 nm for the single layer to 0.52 nm for the bilayer film obtained from the STM measurements, line profiles of which are displayed in Figure 2d. Additionally, Figure 2d shows that the deep trenches observed for the single layer are absent for the bilayer film. This same trend can also be seen when many layers of very dilute precursor solution are used. In this case, however, the thickness remains low (<5 nm in the case of 5 × 5 mg g^{-1} layers) and the resulting layers are very smooth with a surface roughness of 0.4 nm (see Figure 2c). The average layer thicknesses of those layers are obtained from the electron densities of the XRR results displayed in Figure 3a assuming a constant density of the IZO material, with all thicknesses being recorded after heat treatment. The obtained density of the amorphous SiO_2 (ρ = 2.30 g cm^{-3}) is used to calibrate the XRR and is in agreement with former work.[15,22,23] The determined oxide thickness was 89.5(5) nm in agreement the nominal layer thickness of 90 nm as stated by the supplier.

Figure 3a shows the reflectivities of a single 30 mg g^{-1} layer, a double 30 mg g^{-1} layer, and a single 100 mg g^{-1} layer. The lines correspond to least-squares curve fitting results which treat the thickness and the density of the IZO film as free fit parameters. The fit procedure was always started from a single homogeneous layer, adding only a minimal number of extra layers to be able to describe the various features of the reflectivity curves. Adjustments to the free parameters were made in a manner consistent with the appearance of the films from scanning electron microscopy (SEM) and secondary ion mass spectroscopy (SIMS). Finally, the film thickness obtained from the fit was compared with values from collaborative techniques such as SEM and white light interferometery (WLI) to check the validity of the extracted electron density (see Figure S2 and Table T1 in Supporting Information). From the single oscillation frequency of the 100 mg g^{-1} layer, the film thickness can be deduced, while the critical angle of the total reflection is related to the average density of the film. The reflectivity curve cannot be fitted with such a single layer,

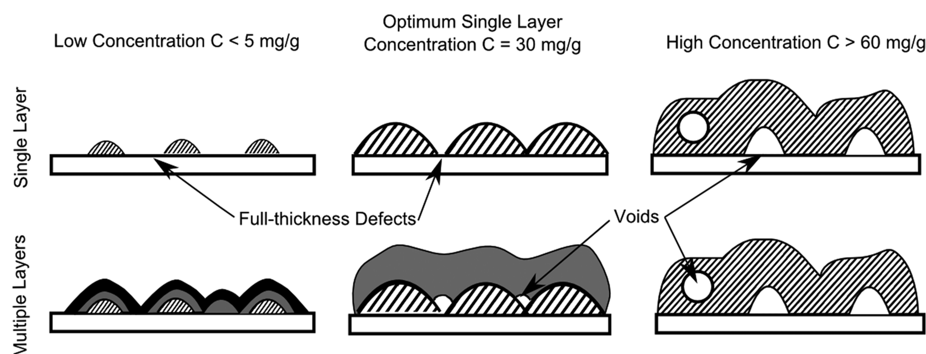

Figure 4. Diagram of mechanism suggested explaining single and multilayer film properties.

neither with an added denser top or bottom layer. The simplest system with a reasonable fit contains both top and bottom interfaces (see the normalized ED profile on Figure 3b). The obtained total thickness of the IZO film of 30.19(4) nm, defined as the sum of the thickness of all IZO layers not taking into account the roughness, is in reasonable agreement with the SEM and WLI result of 25 nm, as shown in the Supporting Information. Note that the obtained electron density of the homogeneous middle part is only 0.506 times the ideal bulk electron density of IZO (see Supporting Information), with an absolute error on the order of 1%.

The 30 mg g^{-1} single layer IZO film in Figure 3a could also not be described by a single homogeneous layer. This is evident from the features of the reflectivity curve. The deep oscillations suggest a large contrast in ED, while the exponential decay after the critical angle with no curvature suggests an ED very similar to the substrate for at least part of the film. For a reasonable match, a second IZO layer had to be introduced in the simulation. First, a denser IZO layer was positioned on the bottom interface and a fit with a total film thickness of 7.08(3) nm and peak density of 0.946 of the ideal bulk value was possible (Figure 3a red curve). Fitting with a model, where the denser IZO layer was positioned on top also gave a good simulation results (Figure 3a green curve). Here, the total film thickness was 7.16(3) nm and the peak density is 0.809 of the ideal bulk IZO value. This latter "mirrored" structure gave a 30% smaller figure of merit (FOM). Although the FOM is slightly lower for the top denser film, this profile makes less sense when considered with the STM images which show valley type features, indicating more material at the substrate than at the top of the film. This cannot be a firm conclusion, however, as the STM reproduces topography and does not account for the internal structure of the layer. For the double 30 mg g^{-1} film in Figure 3a, a good fit with two layers was not possible, and finally, five layers were required to describe the bilayer structure with three interfaces. The total thickness obtained from the fits was 12.48(2) nm. Altogether, we find that the films discussed above have a significantly lower average density than expected for the ideal IZO bulk except for the 5 times 5 mg g^{-1} film (Figure 3b). Moreover, the data in Figure 3b suggests an increase of the average film density with a decreasing precursor concentration. This conclusion is corroborated by Figure 3c which indicates the changes in the ED due to an extra layer of 5 mg g^{-1} on top of a 30 mg g^{-1} layer where an overall increase of the ED is observed upon deposition of the second layer, independently of the applied model, whereas the layer thickness does not change. The ED profiles can be understood by assuming island growth mode with incomplete coverage in case of the first deposition (single film) and the gradual filling of the voids for the second deposition (double film).

The combination of STM and XRR measurements affords the development of a qualitative picture of the mechanism behind the significant increase in mobility observed for multilayer devices. The first layer starts to grow via an island growth mechanism. At concentrations of less than 5 mg g^{-1} precursor, the islands are not sufficiently large to form a continuous percolation pathway across a 20 μm channel, and therefore, the corresponding thin film transistors do not function. Devices with a shorter channel length of 2.5 μm do work well at this concentration, with an extracted mobility of 1.3×10^{-3} cm^2 V^{-1} s^{-1}, supporting the island growth, percolation pathway mechanism.

As shown in Figure 2, for a single layer film, there remain areas of full film thickness variation where there is no IZO material and consequently no electron propagation in case of a field effect transistor (FET), reducing measured mobility. Coating a second thin film bridges these areas, increasing the measured mobility; however, the XRR shows that the second film does not coat all the way to the SiO_2 surface. Hence, small voids in the film remain at the dielectric interface. An attempt was made to improve this situation by coating multiple layers at different spin speeds and precursor concentrations. All films show a peak in the measured mobility after a certain number of deposited layers (Figure 1b), although the absolute value of that peak can vary significantly. Altering the spin speed for a given concentration has a small effect, with higher spin speeds (thinner layers) achieving a slightly higher mobility. Varying the concentration of precursor has a dramatic effect on the maximum mobility, with lower concentrations reaching higher mobilities, however, requiring a higher number of layers to do so. There is a correlation between the inverse of the precursor concentration and the number of layers required to reach this mobility maximum, allowing one to predict how many layers will be required for a given concentration of precursor (Figure 1b inset). It is suspected that the reason for this correlation is simply that, the lower the concentration of precursor, the more layers will be required to result in a complete film that is free of the full thickness variations.

A consistent picture of layer formation in precursor-derived IZO films is shown in Figure 4. The first row of figures show a schematic of the single layer formation process for three concentrations: too low to form a continuous path, the optimum single layer concentration, and high concentrations, which exhibit reduced charge carrier mobilities. The second row of figures shows what is believed to happen upon the

application of further layers up until the point where additional layers make no further improvement. Note that coating additional layers after this optimum point does not increase the mobility but can raise the off current as discussed in relation to Figure 1. The optimum formulation concentration for single layer films is not the optimum for multilayer films, and this is attributed to the presence of voids at the dielectric interface, shown experimentally by the XRR. The multiple layers of low concentration films have been shown to be absent of voids and result in high mobilities.

To further consider why the absence of voids results in extracting a higher mobility, one can turn to the Shockley equations shown in the Experimental Section, eqs 1 and 2. In both cases, the equations are composed of two parts: a geometric prefactor determined by the physical geometry of the device and the current−voltage relation. Since in all cases the voltages applied were identical and it is not thought that the charge carrier mobility in the material itself changes, it must be one or more components in the geometric prefactor that change, affording the higher currents. In fact, the presence of voids can conceivably impact all of these components in such a way that the extracted mobility is lowered. The width available for charge injection is reduced by voids; the length the charges must travel through the available percolation pathways is increased, and the area available to accumulate charge is reduced. Therefore, the effective width and capacitance are lower and the effective length higher than assumed, resulting in a deflated value of the extracted mobility. This mobility, it should be stressed, is an extracted mobility for the device according to the Shockley equations, not the actual mobility of the charge carriers in the material itself which, as stated, probably does not alter. Furthermore, when there are many full thickness variations and defects of larger physical size, as in the single 30 mg g^{-1} films, the charges will have to overcome many more rate limiting barriers as they overcome these defects, if indeed they can be overcome. By simply filling in voids or full film thickness defects, the available width and area able to accumulate charge and form a channel is increased and the length the charges must travel decreases, bringing them closer to the physical values assumed when calculating the mobility.

This work also suggests a possibility to further optimize the processing and gain the high mobilities in low numbers of layers if the full thickness defects could be eliminated. It is thought that different coating techniques could play a key role in achieving this goal.

4. CONCLUSIONS

It has been demonstrated that coating multiple subsequent layers of IZO produces a significant increase in effective charge carrier mobility in bottom gate thin film transistors. On the basis of a combination of scanning probe microscopy and specular X-ray reflection techniques, a qualitative model could be developed for the interrelation between charge transport properties and thin film morphology. Particularly, it has been shown that the elimination of full thickness defects and voids which can occur in thicker layers leads to transistors of notably higher performance. The obtained fundamental understanding of the interrelation between the morphology of metal oxide thin films prepared from solution and their charge transport properties allows one to tailor and to optimize the solution-based preparation of TFTs to achieve high charge carrier mobility, compatible with values obtained from sputtered devices.

■ ASSOCIATED CONTENT

Supporting Information

Information detailing the methods of extracting mobility employed throughout the paper. SEM and SIMS data supporting the morphology argumentation and data on the thickness of the active layers characterized by SEM, WLI, and XRR. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Author

*Tel: +49 6151 16-6689. E-mail: walker@e-mat.tu-darmstadt.de.

Present Address

‡Marton Major Technical University of Darmstadt Dept. Materials Science 64287 Darmstadt, Germany.

Author Contributions

The manuscript was written through contributions of all authors.

Notes

The authors declare no competing financial interest.

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■ ABBREVIATIONS

IZO = indium zinc oxide
ZnO = zinc oxide
AFM = atomic force microscopy
STM = scanning tunneling microscopy
XRR = specular X-ray reflectivity
ED = electron density
FOM = figure of merit
SiO_2 = silicon dioxide
SEM = scanning electron microscope
WLI = white light interferometery
FET = field effect transistor
TFT = thin film transistor

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